

I CLAIM:

1 1. A process for forming a polycrystalline
2 semiconductor portion on a substrate, the method
3 comprising the steps of:

4 (a) depositing semiconductor onto the substrate to
5 form a semiconductor layer having an amorphous region;

6 (b) depositing a metal onto the semiconductor layer
7 to form a structure comprising the substrate,
8 semiconductor layer and a doping metal layer;

9 (c) annealing the structure at a temperature in the
10 range of about 170°C to about 600°C to convert at least
11 a portion of the amorphous region into polycrystalline
12 semiconductor.

1 2. The process of claim 1 wherein the semiconductor
2 comprises at least one selected from the group consisting
3 of silicon, germanium, silicon-germanium alloys,
4 germanium-carbon alloys, silicon-carbon alloys, and
5 silicon-nitrogen alloys.

1 3. The process of claim 2 wherein the semiconductor
2 comprises at least one selected from the group consisting

3 of silicon, germanium and silicon-germanium alloys.

1 4. The process of claim 2 wherein the semiconductor
2 comprises silicon.

1 5. A process for forming a polycrystalline
2 semiconductor layer on a substrate, wherein the substrate
3 comprises a semiconductor layer thereon having an
4 amorphous region, and comprises a metal layer supported
5 on the amorphous semiconductor layer, the method
6 comprising the step of:

7 (a) annealing the structure at a temperature in the
8 range of about 170°C to about 600°C to convert at least
9 a portion of the amorphous region into polycrystalline
10 semiconductor.

1 6. The process of claim 5 wherein the semiconductor
2 comprises at least one compound selected from the group
3 consisting of silicon, germanium, silicon-germanium
4 alloys, germanium-carbon alloys, silicon-carbon alloys,
5 and silicon-nitrogen alloys.

1 7. The process of claim 6 wherein the semiconductor

2 comprises at least one selected from the group consisting
3 of silicon, germanium and silicon-germanium alloys.

1 8. The process of claim 6 wherein the semiconductor
2 comprises silicon.

1 9. Polycrystalline semiconductor comprising greater
2 than about 1×10^{20} aluminum atoms per cm^3 of silicon.

1 10. In a process for manufacturing a semiconductor
2 device, the improvement of forming a semiconductor junction
3 by a method comprising:
4 (a) providing a semiconductor substrate;
5 (b) depositing a layer of amorphous silicon onto said
6 semiconductor substrate to form a structure comprising the
7 semiconductor substrate and the layer of amorphous silicon;
8 (c) depositing a layer of metal onto said layer of
9 amorphous silicon to form a structure comprising the
10 semiconductor substrate, the layer of amorphous silicon,
11 and the layer of metal; and
12 (d) without depositing any additional layers onto the
13 metal layer, annealing the structure formed in step (c) at
14 a temperature in the range of about 170°C to about 600°C to
15 convert at least a portion of the amorphous silicon layer
16 into crystalline silicon, wherein the metal promotes the
17 conversion of the at least a portion of the amorphous
18 region into the crystalline silicon to provide a
19 semiconductor junction between said crystalline silicon and
20 said semiconductor substrate.

1 11. The process of Claim 10, wherein said
2 semiconductor substrate is doped with a dopant of a first

3 conductivity type and said layer of amorphous silicon is
4 doped with a dopant of a second conductivity type opposite
5 to that of said semiconductor substrate.

1 12. The process of Claim 10, wherein said temperature
2 in step (d) is less than about 450°C.

1 13. The process of Claim 12, wherein said temperature
2 in step (d) is in a range of about 200°C to about 300°C.

1 14. The process of Claim 10, wherein the metal
2 includes a doping metal which serves to promote the
3 conversion of at least a portion of the amorphous silicon
4 layer into the crystalline silicon and to dope the
5 crystalline silicon.

1 15. The process of Claim 14, wherein the doping metal
2 is aluminum.

1 16. The process of Claim 14, wherein the doping metal
2 is effective to convert the at least a portion of the
3 amorphous silicon layer from one n-type, intrinsic, or
4 p-type material 6 to another upon crystallization.

1 17. The process of Claim 16, wherein the doping metal
2 is aluminum.

1 18. The process of Claim 10, wherein said annealing
2 is conducted for an annealing time in the range of about
3 1 second to about 24 hours.

1 19. The process of Claim 18, wherein said annealing
2 is conducted for an annealing time in the range of about
3 30 seconds to about 1 hour.

1 20. The process of Claim 19, wherein said annealing
2 is conducted for an annealing time in the range of about
3 1 minute to about 30 minutes.

1 21. In a process for manufacturing a semiconductor
2 device, the improvement of forming a p-n junction by a
3 method comprising:

4 (a) providing a crystalline silicon semiconductor
5 substrate of a first conductivity type;

6 (b) depositing a layer of amorphous silicon onto said
7 semiconductor substrate to form a structure comprising the
8 semiconductor substrate and the layer of amorphous silicon;

9 (c) depositing a layer of doping metal onto said layer
10 of amorphous silicon to form a structure comprising the
11 semiconductor substrate, the layer of amorphous silicon,
12 and the layer of doping metal, wherein said doping metal is
13 selected to provide a dopant of a second conductivity type
14 opposite to that of the semiconductor substrate; and
15 (d) without depositing any additional layers onto the
16 metal layer, annealing the structure formed in step (c) at
17 a temperature in the range of about 170°C to about 600°C to
18 convert at least a portion of the amorphous silicon layer
19 into crystalline silicon doped with the doping metal,
20 wherein the doping metal promotes the conversion of the at
21 least a portion of the amorphous silicon layer into
22 crystalline silicon so as to provide a semiconductor
23 junction between that crystalline silicon and said
24 crystalline silicon substrate.

1 22. The process of Claim 21, wherein said temperature
2 in step (d) is less than about 450°C.

1 23. The process of Claim 22, wherein said temperature
2 in step (d) is in a range of about 200°C to about 300°C.

1 24. The process of Claim 21 , wherein the doping
2 metal is aluminum.

1 25. The process of Claim 21, wherein the doping metal
2 is effective to convert the at least a portion of the
3 amorphous silicon layer from one of an n-type, intrinsic,
4 or p-type material to another upon crystallization.

1 26. The process of Claim 25, wherein the doping metal
2 is aluminum.

1 27. The process of Claim 21, wherein said annealing
2 is conducted for an annealing time in the range of about
3 1 second to about 24 hours.

1 28. The process of Claim 27, wherein said annealing
2 is conducted for an annealing time in the range of about
3 30 seconds to about 1 hour.

1 29. The process of Claim 28, wherein said annealing
2 is conducted for an annealing time in the range of about
3 1 minute to about 30 minutes.

1 30. A process for making a semiconductor junction,

2 comprising:

3 (a) depositing a semiconductor layer having an

4 amorphous region onto a semiconductor surface;

5 (b) depositing a layer of metal onto the amorphous

6 region of the semiconductor layer to form a structure

7 comprising the semiconductor surface, the semiconductor

8 layer, and the metal layer; and

9 (c) without depositing any additional layers onto the

10 metal layer, annealing the structure formed in step (b) at

11 a temperature in the range of about 170°C to about 600°C so

12 as to convert at least a portion of the amorphous region

13 into a crystalline semiconductor having a junction with the

14 semiconductor surface, wherein the metal of a first portion

15 of the metal layer promotes the conversion of the at least

16 a portion of the amorphous region into the crystalline

17 semiconductor.

1 31. The process of Claim 30, wherein said temperature

2 in step (c) is less than about 450°C.

1 32. The process of Claim 31, wherein said temperature

2 in step (d) is in a range of about 200°C to about 300°C.

1 33. The process of Claim 30, wherein the metal
2 includes a doping metal which serves to promote the
3 conversion of at least a portion of the amorphous region
4 into the crystalline semiconductor and to dope the
5 crystalline semiconductor.

1 34. The process of Claim 33, wherein the doping metal
2 is aluminum.

1 35. The process of Claim 33, wherein the doping metal
2 is effective to convert the at least a portion of the
3 amorphous region from one of an n-type, intrinsic, or p-
4 type material to another upon crystallization.

1 36. The process of Claim 35, wherein the doping metal
2 is aluminum.

1 37. The process of Claim 30, wherein said annealing
2 is conducted for an annealing time in the range of about
3 1 second to about 24 hours.

1 38. The process of Claim 37, wherein said annealing
2 is conducted for an annealing time in the range of about
3 30 seconds to about 1 hour.

1 39. The process of Claim 38, wherein said annealing
2 is conducted for an annealing time in the range of about
3 1 minute to about 30 minutes.

1 40. A process for making a semiconductor junction,
2 comprising:

3 (a) providing a structure including a semiconductor
4 surface, a semiconductor layer having an amorphous region
5 on the semiconductor surface, and a metal outer layer on
6 the amorphous region;

7 (b) annealing the structure provided in step (a) at a
8 temperature in the range of about 170°C to about 600°C so
9 as to convert at least a portion of the amorphous region
10 into a crystalline semiconductor having a junction with the
11 semiconductor surface, wherein the metal of a portion of
12 the metal layer promotes the conversion of the at least a
13 portion of the amorphous region into the crystalline
14 semiconductor.

1 41. The process of Claim 40, wherein said temperature
2 in step (b) is less than about 450°C.

1 42. The process of Claim 41, wherein said temperature
2 in step (b) is in a range of about 200°C to about 300°C.

1 43. The process of Claim 40, wherein the metal
2 includes a doping metal which serves to promote the
3 conversion of the at least a portion of the amorphous
4 region into the crystalline semiconductor silicon and to
5 dope the crystalline semiconductor.

1 44. The process of Claim 43, wherein the doping metal
2 is aluminum.

1 45. The process of Claim 43, wherein the doping metal
2 is effective to convert the at least a portion of the
3 amorphous region from one of an n-type, intrinsic, or p-
4 type material to another upon crystallization.

1 46. The process of Claim 45, wherein the doping metal
2 is aluminum.

1 47. The process of Claim 40, wherein said annealing
2 is conducted for an annealing time in the range of about
3 1 second to about 24 hours.

1 48. The process of Claim 47, wherein said annealing
2 is conducted for an annealing time in the range of about
3 30 seconds to about 1 hour.

1 49. The process of Claim 48, wherein said annealing
2 is conducted for an annealing time in the range of about
3 1 minute to about 30 minutes.

1 50. A process for making a semiconductor junction,
2 comprising:

3 (a) providing a structure including a semiconductor
4 layer having an amorphous semiconductor region disposed
5 thereon, and metal on the amorphous region with no
6 additional layer being formed over the metal;

7 (b) annealing the structure provided in step (a) at a
8 temperature in the range of about 170°C to about 600°C so
9 as to convert at least a portion of the amorphous region
10 into a crystalline semiconductor having a junction with the
11 semiconductor layer, wherein the metal includes a portion

12 that promotes the conversion of the at least a portion of
13 the amorphous region into the crystalline semiconductor.

1 51. The process of Claim 50, wherein said temperature
2 in step (b) is less than about 450°C.

1 52. The process of Claim 51, wherein said temperature
2 in step (b) is in a range of about 200°C to about 300°C.

1 53. The process of Claim 52, wherein the metal
2 includes a doping metal which serves to promote the
3 conversion of the at least a portion of the amorphous
4 region into the crystalline semiconductor and to dope the
5 crystalline semiconductor.

1 54. The process of Claim 53, wherein the doping metal
2 is aluminum.

1 55. The process of Claim 53, wherein the doping metal
2 is effective to convert the at least a portion of the
3 amorphous region from one of an n-type, intrinsic, or p-
4 type material to another upon crystallization.

1 56. The process of Claim 55, wherein the doping metal
2 is aluminum.

1 57. The process of Claim 50, wherein said annealing
2 is conducted for an annealing time in the range of about
3 1 second to about 24 hours.

1 58. The process of Claim 57, wherein said annealing
2 is conducted for an annealing time in the range of about
3 30 seconds to about 1 hour.

1 59. The process of Claim 58, wherein said annealing
2 is conducted for an annealing time in the range of about
3 1 minute to about 30 minutes.

1 60. A structure for use in manufacturing a
2 semiconductor device consisting of :
3 (a) a lower single crystalline silicon substrate;
4 (b) an intermediate amorphous silicon semiconductor
5 layer in contact with said single crystalline silicon
6 substrate; and
7 (c) an uppermost metal layer in contact with said
8 amorphous silicon semiconductor layer.

1 61. A structure for use in manufacturing a
2 semiconductor device consisting of comprising:
3 (a) a lower single crystalline silicon substrate;
4 (b) an intermediate polycrystalline silicon
5 semiconductor layer in contact with said single crystalline
6 silicon substrate;
7 (c) an uppermost metal layer in contact with said
8 polycrystalline silicon semiconductor layer.

1 62. A semiconductor device consisting of :
2 (a) a lower single crystalline silicon substrate of a
3 first conductivity type;
4 (b) an intermediate polycrystalline silicon layer in
5 contact with said single crystalline silicon substrate,
6 said polycrystalline silicon layer having a second
7 conductivity type opposite to that of said single
8 crystalline silicon substrate; and
9 (c) an uppermost metal layer in contact with said
10 intermediate polycrystalline silicon layer.